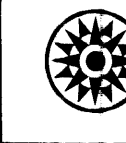


The IBM logo, consisting of the letters "IBM" in a bold, sans-serif font, is positioned on a dark, textured rectangular background.

Systems Reference Library

System/360 Instruction Timing Information

This bulletin contains instruction timing information for all models of the System/360. For a full description of each instruction, refer to IBM System/360 Principles of Operation, Form A22-6821.



MAJOR REVISION (May 1964)

This publication, Form A22-6825-1, obsoletes
Form A22-6825-0, N22-0133, and N22-0135.

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SYSTEM/360 INSTRUCTION TIMING INFORMATION

The instruction time tables presented in this bulletin provide average instruction times, in microseconds, for all models of the IBM System/360. All times for instructions that reference storage include the time required to perform single indexing by one general register as referenced in the instruction (i.e., $B \neq 0$). For those instructions in which indexing may be performed two times (i.e., all RX format instructions), the time required for the second indexing must be added to the basic time given in the table, as follows:

MODEL	ADDITIONAL TIME (in microseconds)
30	6.0
40	1.25
50	0.5
60	0.125
62	0.125
70	0.0

The instructions that may be indexed a second time are highlighted by an asterisk in the table.

TIMING CONDITIONS

The following conditions were used in the development of these instruction time tables.

1. All instruction timings pertain only to storage references to main storage as follows:

MODEL	SPEED (in microseconds)	WIDTH (in bytes)
30	2.0	1
40	2.5	2
50	2.0	4
60	2.0*	8
62	1.0	8
70	1.0*	8

* Interleaved. Provides reduced access time for consecutively addressed references by overlapping storage cycles of odd and even addresses.

2. In all storage operations, positive and negative operands are equally probable.
3. Each bit location has equal probability for the binary values 0 or 1, and each bit location is independent of other bit locations. Decimal data may contain digit values 0 to 9 in each digit position with equal probability.
4. Variable field length instructions may start on even or odd halfwords with equal probability.
5. Interruptions or masked-off program exceptions are not reflected in these timings.

TIMING ASSUMPTIONS

The following assumptions were used in the development of these instruction time tables.

1. For decimal-add and decimal-subtract instructions, the first operand (i.e., the destination field) is assumed to be greater than, or equal to, the length of the second operand (i.e., the source field).
2. For decimal-add and decimal-subtract instructions, recomplementation time is not included in the times given.
3. In the EDIT AND MARK (EDMK) instruction, an address is stored once. That is, this instruction is used with a single field, or a line with only one numeric field rather than a complete print line.
4. In the TRANSLATE AND TEST (TRT) instruction, it is assumed that a non-zero byte from the Translate and Test table is found.
5. The instruction times for the floating-point instructions depend upon the number of hexadecimal digits that are preshifted and postshifted, as well as the number of times recomplementation of a result occurs. The times given in the instruction time tables for floating-point instructions are a weighted average of these variables.

SYSTEM / 360								
INSTRUCTION	FORMAT	MNEMONIC	MODEL					
			30	40	50	60	62	70
			Time B ≠ 0	Time B ≠ 0	Time B ≠ 0	Time B ≠ 0	Time B ≠ 0	Time B ≠ 0
Add	RR	AR	29.	7.5	3.25	1.0	.84	.4
Add *	RX	A	39.	11.88	4.0	2.81	1.87	1.05
Add Decimal	SS	AP	See Table AP					
Add Halfword *	RX	AH	37.	10.94	5.5	3.44	2.37	1.12
Add Logical	RR	ALR	30.	7.5	3.25	1.0	.84	.4
Add Logical *	RX	AL	40.	11.88	4.0	2.81	1.87	1.05
Add Normalized (Long)	RR	ADR	105.	22.53	7.84	2.35	2.19	.85
Add Normalized (Long) *	RX	AD	115.	27.66	9.69	4.05	3.22	1.13
Add Normalized (Short)	RR	AER	65.	14.3	6.13	2.33	2.17	.85
Add Normalized (Short) *	RX	AE	75.	18.66	6.88	4.03	3.20	1.13
Add Unnormalized (Long)	RR	AWR	88.	20.86	7.15	2.29	2.13	.90
Add Unnormalized (Long) *	RX	AW	98.	25.99	9.00	3.99	3.16	1.15
Add Unnormalized (Short)	RR	AUR	56.	13.59	5.38	2.26	2.10	.9
Add Unnormalized (Short) *	RX	AU	66.	17.95	6.13	3.96	3.13	1.15
AND	RR	NR	30.	7.5	5.0	1.75	1.59	.6
AND *	RX	N	40.	11.88	5.75	3.44	2.62	1.08
AND	SI	NI	20.	9.38	6.5	4.18	2.43	2.2
AND	SS	NC	See Table NC					
Branch and Link	RR	BALR	B 24. NB 19.	B 8.75 L 6.88	B 4.25 NB 3.0	2.25	1.53	1.0
Branch and Link *	RX	BAL	35.	11.88	4.5	2.40	1.53	1.0
Branch on Condition	RR	BCR	B 14. NB 9.	B 5.01 NB 4.39	B 3.75 NB 2.75	B 2.25 NB 1.00	B 1.53 NB .84	1.0
Branch on Condition *	RX	BC	B 22. NB 21.	9.38	B 4.0 NB 3.0	B 2.40 NB 1.37	B 1.53 NB 1.00	1.0
Branch on Count	RR	BCTR	B 19.-27. NB 25. C ₁ 14.-22.	B 8.13 NB 8.76 C ₁ 6.88	B 4.75 NB 3.75	B 2.25 NB 1.84	B 1.53 NB 1.44	1.0
Branch on Count *	RX	BCT	B 24.-32. NB 30.	B 10.63 NB 11.26	B 4.5 NB 3.5	B 2.40 NB 2.93	B 1.53 NB 1.62	1.0
Branch on Index High	RS	BXH	B 52. NB 51.	16.26	B 5.5 NB 4.5	B 2.25 NB 2.87	B 1.75 NB 2.00	1.1
Branch on Index Low or Equal	RS	BXLE	B 52. NB 51.	16.26	B 5.5 NB 4.5	B 2.25 NB 2.87	B 1.75 NB 2.00	1.1
Compare	RR	CR	26.	7.5	3.25	1.0	.84	.4
Compare *	RX	C	39.	11.88	4.0	2.81	1.87	1.05
Compare Decimal	SS	CP	See Table CP					
Compare Halfword *	RX	CH	36.	9.38 to 11.25	6.0	3.44	2.37	1.12
Compare Logical	RR	CLR	16.to 26.	7.5	3.0	1.0	.84	.4
Compare Logical *	RX	CL	26.to 36.	11.88	4.0	2.81	1.87	1.05

Time shown in microseconds.

Note: Legend for this chart on page 8

INSTRUCTION	FORMAT	MNEMONIC	30	40	50	60	62	70
Compare Logical	SI	CLI	20.	9.38	4.5	2.81	1.87	1.12
Compare Logical	SS	CLC	See Table CLC					
Compare (Long)	RR	CDR	87.	19.21	6.59	1.79	1.63	.8
Compare (Long) *	RX	CD	97.	24.33	8.39	3.48	2.66	1.12
Compare (Short)	RR	CER	55.	11.74	5.36	1.76	1.60	.8
Compare (Short) *	RX	CE	65.	16.38	6.11	3.45	2.63	1.12
Convert to Binary *	RX	CVB	115. to 380.	31.88 to 87.81	12.75 to 43.25	10.43	9.62	3.8
Convert to Decimal *	RX	CVD	57. to 381.	28.15 to 98.75	14.75 to 44.75	P-10.69 N-11.19	P-9.87 N-10.37	8-.8C + .2D
Divide	RR	DR	550.	175.00 to 192.50	33	10.62	10.46	5.5
Divide *	RX	D	560.	176.88 to 196.88	33.25	11.93	11.2	5.7
Divide Decimal	SS	DP	See Table DP					
Divide (Long)	RR	DDR	2500	472.5	68.75	16.75	16.59	7.3
Divide (Long) *	RX	DD	2510.	476.88	69.5	18.43	17.62	7.3
Divide (Short)	RR	DER	600.	128.13	22.25	8.25	8.10	4.1
Divide (Short) *	RX	DE	610.	132.5	23.0	9.93	9.12	4.1
Edit	SS	ED	See Table ED					
Edit and Mark	SS	EDMK	See Table EDMK					
Exclusive OR	RR	XR	30.	7.5	5.0	1.75	1.59	.6
Exclusive OR *	RX	X	40.	11.88	5.75	3.44	2.62	1.08
Exclusive OR	SI	XI	21.	9.38	6.5	4.18	2.43	2.2
Exclusive OR	SS	XC	See Table XC					
Execute *	RX	EX	25. + ED	8.76 +EO	5.75 +EO	4.75 +EO	2.49 +EO	3.2 +EO
Halt I/O	SI	HIO	55 + CRT	M 35 + CRT S 20-63 + CRT	8.75 + CRT	2.19 + CRT	1.87 + CRT	CRT
Halve (Long)	RR	HDR	102.	12.5	4.25	1.75	1.59	.4
Halve (Short)	RR	HER	50.	7.5	3.25	1.50	1.34	.4
Insert Character *	RX	IC	21.	9.38	5.0	2.81	1.87	1.12
Insert Storage Key	RR	ISK	18.	8.13	5.25	2.75	2.09	1.48
Load	RR	LR	22	7.5	2.5	1.0	.84	.4
Load *	RX	L	32.	11.88	4.0	2.69	1.62	1.05
Load Address *	RX	LA	25.	10.0	2.75	1.43	1.12	1.08
Load and Test	RR	LTR	28.	7.5	2.5	1.0	.84	.4
Load and Test (Long)	RR	LTDR	42.	12.5	4.0	1.50	1.34	.4
Load and Test (Short)	RR	LTER	25.	7.5	3.25	1.25	1.09	.4
Load Complement	RR	LCR	28.	7.5	2.75	1.0	.84	.4
Load Complement (Long)	RR	LCDR	42.	12.5	4.0	1.50	1.34	.4
Load Complement (Short)	RR	LCER	25.	7.5	3.25	1.25	1.09	.4
Load Halfword *	RX	LH	28.	10.63	4.75	3.19	2.12	1.12
Load (Long)	RR	LDR	39	12.5	3.5	1.50	1.34	.4
Load (Long) *	RX	LD	49	16.88	5.25	2.81	1.87	1.05

Time shown in microseconds

Note: Legend for this chart on page 8

INSTRUCTION	FORMAT	MNEMONIC	30	40	50	60	62	70
Load Multiple	RS	LM	16. + 16 R	6.25 + 5R	3 + 2R	1.43 + 1.25 B ₁	1.12 + B ₁	1.4 + .26R
Load Negative	RR	LNR	28.	7.5	2.88	1.37	1.21	.4
Load Negative (Long)	RR	LNDR	42.	12.5	4.0	1.50	1.34	.4
Load Negative (Short)	RR	LNER	25.	7.5	2.75	1.25	1.09	.4
Load Positive	RR	LPR	28.	7.5	3.0	1.37	1.21	.4
Load Positive (Long)	RR	LPDR	42.	12.5	4.0	1.50	1.34	.4
Load Positive (Short)	RR	LPER	25.	7.5	2.75	1.25	1.09	.4
Load PSW	SI	LPSW	37.	16.25	8.0	2.81	1.87	3.1
Load (Short)	RR	LER	23.	7.5	2.25	1.0	.84	.4
Load (Short) *	RX	LE	33.	11.88	3.25	2.69	1.62	1.05
Move	SI	MVI	18.	9.38	4.5	2.93	1.93	1.46
Move	SS	MVC	See Table MVC					
Move Numerics	SS	MVN	See Table MVN					
Move with Offset	SS	MVO	See Table MVO					
Move Zones	SS	MVZ	See Table MVZ					
Multiply	RR	MR	304.	83.28	27.5	5.75	5.59	2.8
Multiply *	RX	M	313.	84.72	28.75	6.93	6.12	2.8
Multiply Decimal	SS	MP	See Table MP					
Multiply Halfword *	RX	MH	100.	45.	21.75	7.43	6.62	3.2
Multiply (Long)	RR	MDR	1050.	255.	37.75	9.25	9.09	4.2
Multiply (Long) *	RX	MD	1060.	259.38	38.0	10.44	9.62	4.2
Multiply (Short)	RR	MER	310.	76.25	20.75	5.25	5.09	2.2
Multiply (Short) *	RX	ME	320.	80.63	21.5	6.93	6.12	2.2
OR	RR	OR	30.	7.5	5.0	1.75	1.59	.6
OR *	RX	O	40.	11.88	5.75	3.44	2.62	1.08
OR	SI	OI	21.	9.38	6.5	4.18	2.43	2.2
OR	SS	OC	See Table OC					
Pack	SS	PACK	See Table PACK					
Read Direct	SI	RDD	24 + ED	12.5 + ED	6.5 + ED	2.70 + ED	2.37 + ED	1.86 + ED
Set Program Mask	RR	SPM	13.	5.0	2.75	1.0	.84	.8
Set Storage Key	RR	SSK	19.	8.13	4.75	2.5	1.84	1.46
Set System Mask	SI	SSM	21.	10.0	5.5	3.19	2.37	1.12
Shift Left Double	RS	SLDA	See Shift Tables					
Shift Left Double Logical	RS	SLDL	See Shift Tables					
Shift Left Single	RS	SLA	See Shift Tables					
Shift Left Single Logical	RS	SLL	See Shift Tables					
Shift Right Double	RS	SRDA	See Shift Tables					
Shift Right Double Logical	RS	SRDL	See Shift Tables					
Shift Right Single	RS	SRA	See Shift Tables					

Time shown in microseconds

Note: Legend for this chart on page 8

INSTRUCTION	FORMAT	MNEMONIC	30	40	50	60	62	70	
Shift Right Single Logical	RS	SRL	See Shift Tables						
Start I/O	SI	SIO	120.+ CRT	M 76.25 + CRT S 65.0 + CRT	10.75 + CRT	2.19 + CRT	1.87 + CRT	CRT	
Store *	RX	ST	32.	12.5	4.0	2.37	1.44	1.26	
Store Character *	RX	STC	21.	10.0	4.5	2.87	1.94	1.46	
Store Halfword *	RX	STH	25.	10.0	5.0	3.37	2.44	1.46	
Store (Long) *	RX	STD	49.	17.5	5.75	2.37	1.44	1.26	
Store Multiple	RS	STM	17 + 16R	6.87+ 5R	3 + 2R	1.18 + 1.25 I	.62 + I	1.46 + .2R	
Store (Short) *	RX	STE	33.	12.5	3.75	2.37	1.44	1.26	
Subtract	RR	SR	29.	7.5	3.25	1.0	.84	.4	
Subtract *	RX	S	39.	11.88	4.0	2.81	1.87	1.05	
Subtract Decimal	SS	SP	See Table SP						
Subtract Halfword *	RX	SH	37.	10.94	5.5	3.19	2.12	1.12	
Subtract Logical	RR	SLR	30.	7.5	3.25	1.0	.84	.4	
Subtract Logical *	RX	SL	40.	11.88	4.0	2.81	1.87	1.05	
Subtract Normalized (Long)	RR	SDR	105.	22.53	7.84	2.35	2.19	.85	
Subtract Normalized (Long) *	RX	SD	115.	27.66	9.69	4.05	3.22	1.13	
Subtract Normalized (Short)	RR	SER	65.	14.3	6.13	2.33	2.17	.85	
Subtract Normalized (Short) *	RX	SE	75.	18.66	6.88	4.03	3.20	1.13	
Subtract Unnormalized (Long)	RR	SWR	88.	20.86	7.15	2.29	2.13	.9	
Subtract Unnormalized (Long) *	RX	SW	98.	25.99	9.0	3.99	3.16	1.15	
Subtract Unnormalized (Short)	RR	SUR	56.	13.59	5.38	2.26	2.10	.9	
Subtract Unnormalized (Short) *	RX	SU	66.	17.95	6.13	3.96	3.13	1.15	
Supervisor Call	RR	SVC	58.	23.75	12.75	6.95	4.59	3.8	
Test Channel	SI	TCH	40 + CRT	M-11.25 + CRT S-12.5 + CRT	6.5 + CRT	2.19 + CRT	1.87 + CRT	CRT	
Test I/O	SI	TIO	110 + CRT	See Table TIO	9.25 + CRT	2.19 + CRT	1.87 + CRT	CRT	
Test Under Mask	SI	TM	21.	9.38	5.5	3.19	2.37	1.08	
Translate	SS	TR	See Table TR						
Translate and Test	SS	TRT	See Table TRT						
Unpack	SS	UNPK	See Table UNPK						
Write Direct	SI	WRD	22.	9.37	7.0	3.44	2.62	1.28	
Zero and Add	SS	ZAP	See Table ZAP						

Time shown in microseconds

Note: Legend for this chart on page 8

TIO Table		
Multiplexor Channel		Selector Channel
26.88 + 1.25 a	Unit free or busy Subchannel not busy *	Same as Multiplexor Channel
46.88 + 1.25 a	Interrupt in unit Subchannel not busy *	Same as Multiplexor Channel
50.00 + 1.25 a	End Interrupt in U C W. Subchannel busy.	36.88 + 1.25 a End interrupt in U C W. Subchannel busy.
60.00 + 1.25 a	End in unit Subchannel busy *	
16.25 + 1.25 a	Subchannel busy with other unit	Same as Multiplexor Channel
* Plus up to 32 microseconds interface delay. a = 1 if B ≠ 0, otherwise a = 0		

Legend	
B	= Branch
NB	= No Branch
C ₁	= Count only
L	= Link only
P	= Positive
N	= Negative
C	= number of high order zero digits (hexadecimal) in operand
D	= number of normalization cycles required.
EO	= Executed Operation
CRT	= Channel Response Time
M	= Multiplexor Channel
S	= Selector Channel
R	= number of registers loaded or stored
B ₁	= number of 64 bit transfers
ED	= External Delay
* Indicates double indexing capability	

AP-ADD Decimal	
MODEL	
30	$60 + 5 N_1$
40	$29.35 + 3.75 N_1$
50	$12.8 + 2.4 N_1$
60	$5.28 + .66 N_1 + .25 N_2$
62	$4.15 + .50 N_1 + .13 N_2$
70	$4.20 + .35 N_1 + .05 N_2$
NG-AND	
MODEL	
30	$43 + 5 N$
40	$16.25 + 3.13 N$
50	$12.33 + 1.63 N$
60	$5.25 + .91 N$
62	$3.40 + .66 N$
70	$3.60 + .40 N$
CP-Compare Decimal	
MODEL	
30	$60 + 5 M$
40	$25.0 + 2.5 M$
50	$14.62 + .37 N_1 + .50 N_2 + 1.25 M + .50 D$
60	$5.44 + .25 (N_1 + N_2 + M)$
62	$4.12 + .125 (N_1 + N_2 + 2 M)$
70	$4.00 + .20 M + .15 N_1 + .05 N_2$
CLC-Compare Logical	
MODEL	
30	$43 + 5 B$
40	$15.63 + 2.81 B$
50	$10.25 + 1.0 B$
60	$5.4 + .75 B$
62	$3.56 + .50 B$
70	$4.2 + .40 B$
DP-Divide Decimal	
MODEL	
30	$12 + 3 N_1 + (N_1 - N_2) (71.5 N_2 + 110.5) - 32 N_2$
40	$20.63 + 51.57 N_1 - 40.94 N_2 + 11.25 N_2 (N_1 - N_2)$
50	$23.88 + 8.25 N_1 - 6.88 N_2 + \alpha [7.88 (N_1 - N_2) + 1.13]$
60	$12.46 + 7.60 N_1 - 6.06 N_2 + 2.75 N_2 (N_1 - N_2)$
62	$11.17 + 7.53 N_1 - 6.13 N_2 + 2.75 N_2 (N_1 - N_2)$
70	$4.86 + 3.47 N_1 - 3.74 N_2 + 1.68 N_2 (N_1 - N_2)$
ED - EDIT	
MODEL	
30	$50 + 9 N_1 + 11 N_2$
40	$21.58 + 3.12 N_1 + 1.96 N_2 + 1.25 F - 1.56 K$
50	$8.88 + 2.38 N_1 + .5 N_2 + .5K$
60	$5.21 + 1.19 N$
62	$3.37 + .94 N$
70	$3.9 + .50 N$
EDMK-Edit and Mark	
MODEL	
30	$60 + 9 N_1 + 11 N_2$
40	$24.08 + 3.12 N_1 + 1.96 N_2 + 1.25 F - 1.56 K$
50	$9.38 + 2.38 N_1 + .5 N_2 + .5 K$
60	$7.21 + 1.19 N$
62	$4.87 + .95 N$
70	$4.9 + .5 N$

XC-Exclusive OR	
MODEL	
30	$43 + 5 N$
40	$16.25 + 3.13 N$
50	$12.33 + 1.63 N$
60	$5.25 + .91 N$
62	$3.40 + .66 N$
70	$3.6 + .4 N$
MVC-Move Characters	
MODEL	
30	$40 + 4 N$
40	$16.25 + 2.5 N$
50	$11.33 + 1.13 N$
60	$5.53 + .85 N$
62	$3.81 + .47 N$
70 (Bytes)	$4.00 + .40 N$
70 (Double Words)	$2.2 + 1.6 W$
MVN-Move Numerics	
MODEL	
30	$40 + 5 N$
40	$15.63 + 3.75 N$
50	$12.33 + 1.63 N$
60	$5.25 + .91 N$
62	$3.40 + .66 N$
70	$3.60 + .40 N$
MVO-Move with Offset	
MODEL	
30	$41 + 3 (N_1 + N_2)$
40	$19.37 + 3.13 N_1 + 5.0 N_2$
50	$11.25 + 1.38 N_1 + .63 N_2$
60	$5.5 + .63 N_1 + .28 N_2$
62	$3.56 + .59 N_1 + .16 N_2$
70	$3.85 + .30 N_1 + .05 N_2$
MVZ-Move Zones	
MODEL	
30	$40 + 5 N$
40	$15.63 + 3.75 N$
50	$12.33 + 1.63 N$
60	$5.25 + .91 N$
62	$3.40 + .66 N$
70	$3.60 + .40 N$
MP-Multiply Decimal	
MODEL	
30	$45 + 54 N_1 - 54 N_2 + 28 N_2 (N_1 - N_2)$
40	$25.58 + 21.81 N_1 - 17.84 N_2 + 3.75 N_2 (N_1 - N_2)$
50	$20.80 + 6.4 N_1 - 4.15 N_2 + \alpha [6 (N_1 - N_2) + 1.5]$
60	$8.47 + 3.78 N_1 - 2.31 N_2 + 1.25 N_2 (N_1 - N_2)$
62	$7.17 + 3.72 N_1 - 2.37 N_2 + 1.25 N_2 (N_1 - N_2)$
70	$2.4 + 2.45 N_1 - .47 N_2 + N_2 (N_1 - N_2)$
OC-OR	
MODEL	
30	$43 + 5 N$
40	$16.25 + 3.13 N$
50	$12.33 + 1.63 N$
60	$5.25 + .91 N$
62	$3.40 + .66 N$
70	$3.60 + .40 N$

Note: Legend for this chart on page 10

PACK-PACK	
MODEL	
30	$41 + 3 (N_1 + N_2)$
40	$18.12 + 3.12 N_1 + 1.88 N_2$
50	$10.75 + .88 N_1 + .88 N_2$
60	$5.50 + .63 N_1 + .28 N_2$
62	$3.56 + .59 N_1 + .16 N_2$
70	$3.65 + .50 N_1 + .05 N_2$
SP-Subtract Decimal	
MODEL	
30	$60 + 5 N_1$
40	$29.35 + 3.75 N_1$
50	$12.8 + 2.4 N_1$
60	$5.28 + .66 N_1 + .25 N_2$
62	$4.15 + .5 N_1 + .13 N_2$
70	$4.2 + .35 N_1 + .05 N_2$
TR-Translate	
MODEL	
30	$41 + 7 N$
40	$17.50 + 6.25 N$
50	$6.75 + 4.5 N$
60	$5.24 + 3.66 N$
62	$3.34 + 2.47 N$
70	$4.00 + 1.40 N$
TRT-Translate and Test	
MODEL	
30	$51 + 8 B$
40	$20.0 + 3.75 B$
50	$7.38 + 4.38 B$
60	$7.18 + 4.22 B$
62	$4.71 + 2.59 B$
70	$4.60 + 1.40 B$
UNPK-Unpack	
MODEL	
30	$41 + 3 (N_1 + N_2)$
40	$18.75 + 3.12 N_1 + 2.50 N_2$
50	$10.12 + 1.12 N_1 + .38 N_2$
60	$5.4 + .69 N_1 + .31 N_2$
62	$3.43 + .69 N_1 + .19 N_2$
70	$3.65 + .3 N_1 + .05 N_2$
ZAP-Zero and Add	
MODEL	
30	$57 + 5 N_1$
40	$25.62 + 2.5 N_1$
50	$11.75 + 1.13 N_1 + .37 N_2$
60	$4.91 + .53 N_1 + .25 N_2$
62	$3.81 + .34 N_1 + .13 N_2$
70	$4.25 + .30 N_1 + .05 N_2$
Where:	
N = Total number of bytes in field.	
N ₁ = Total number of bytes in first operand	
N ₂ = Total number of bytes in second operand	
M = Maximum of N ₁ and N ₂ .	
K = Total number of control characters in edit pattern.	
B = Total number of bytes processed.	
D = Absolute value (i.e., unsigned integer value of N ₁ - N ₂)	
W = Total number of double words in field.	
α = 0 if N ₂ ≤ 4	
α = 1 if N ₂ > 4.	
F = Total number of field separator characters in edit pattern.	

SHIFT TABLES

MODEL 30

SLL	58.0 + 5 A
SLDL	98.0 + 10 A
SRL	58.0 + 5 A
SRDL	98.0 + 10 A
SLA	62.0 + 3 B + 5 A
SLDA	104.0 + 3 B + 10 A
SRA	62.0 + 5 A
SRDA	104.0 + 10 A

Where: Bits Modulo
 Left Shift A = 1 for a shift of 3, 4, 5, 6 8
 A = 2 for a shift of 7 8
 A = 0 for a shift of 0, 1, 2 8

Right Shift A = 1 for a shift of 2, 3, 4, 5 8
 A = 2 for a shift of 1 8
 A = 0 for a shift of 0, 6, 7 8

Bits
 B = 0 for a shift of 0 thru 7
 B = 1 " 8 thru 15
 B = 2 " 16 thru 23
 B = 3 " 24 thru 31
 B = 4 " 32 thru 39
 B = 5 " 40 thru 47
 B = 6 " 48 thru 55
 B = 7 " 56 thru 63

MODEL 40

No. of Bits Shifted	Shift Instructions							
	SRL	SLL	SRA	SLA	SRDL	SLDL	SRDA	SLDA
0	11.88	11.25	15.00	16.88	12.50	12.50	18.75	20.63
1	15.00	15.00	18.13	20.63	20.63	18.75	26.88	24.38
2	20.00	19.38	23.13	25.00	27.50	27.50	33.75	28.75
3	15.00	18.13	18.13	23.75	18.13	26.88	24.38	27.50
4	15.00	15.00	18.13	20.63	18.13	18.75	24.38	24.38
5	18.13	15.00	21.25	20.63	26.25	18.75	32.50	24.38
6	20.00	19.38	23.13	25.00	27.50	27.50	33.75	28.75
7	15.00	18.13	18.13	23.75	18.13	26.88	24.38	27.50
8	15.00	15.00	18.13	20.63	18.13	18.75	24.28	24.38
9	18.13	15.00	21.25	20.63	26.25	18.75	32.50	24.38
10	19.38	19.38	22.50	25.00	26.25	27.50	32.50	28.75
11	15.00	18.13	18.13	23.75	19.38	26.88	25.63	27.50
12	15.00	15.00	18.13	20.63	19.38	18.75	25.63	24.38
13	18.75	15.00	21.88	20.63	28.13	18.75	34.38	24.38
14	19.38	19.38	22.50	25.00	26.25	27.50	32.50	28.75
15	15.00	16.25	18.13	21.88	19.38	25.00	25.63	33.13

Extra times for shifts in multiples of 16 bits to be added to shifts less than 16.

16	3.75	3.13	3.75	3.75	7.50	5.63	7.50	6.25
32	6.88	5.63	6.88	6.88	14.38	10.63	14.38	11.88
48	10.00	1.88	10.00	10.00	21.25	15.63	21.25	17.50

Example: (1) SRL of 16 bits = 16 + 0 shifts = 11.88 + 3.75 = 15.63 usec.
 (2) SLDA of 43 bits = 32 + 11 shifts = 11.88 + 27.50 = 39.38 usec.

Note: add .625 usec to total if B ≠ 0.

MODEL 50

SLL	4 + .5 P + .5 Q + .5 S (Q)
SLDL	4 + P + Q + .5 S (Q)
SRL	4 + .5 P + .5 Q + .5 S (Q)
SRDL	4 + P + Q + .5 S (Q)
SLA	4 + .5 P + .5 Q + .5 A + .5 S (Q)
SLDA	5 + P + Q + 26 + .5 (S (Q) (1-C) + .52
SRA	4 + .5 P + .5 Q + .5 S (Q)
SRDA	4 + P + Q + .5 S (P) + .5 S (Q) + .5 Z

Where:
 P = # of 4 bit shifts.
 Q = # of 1 bit shifts.
 Z = 1 if high order part of result is zero; 0 otherwise
 C = 1 if operand is negative; 0 otherwise
 A = 1 if Q ≠ 0 and operand is negative; 0 otherwise
 S (X) is a function defined as S (X) = 1 if X = 0; S (X) = 0 if X ≠ 0

MODEL 60/62

60			62		
SLL	L ₁ , L ₅	1.56	SLL	L ₁ , L ₅	1.12
SLA	L ₂ , L ₆	1.56	SLA	L ₂ , L ₆	1.12
	L ₃ , L ₇ , L ₁₁	1.81		L ₃ , L ₇ , L ₁₁	1.37
	L ₄	1.56		L ₄	1.12
For each additional L ₄ , add .25			For each additional L ₄ , add .25		
SLDL	L ₁	2.31	SLDL	L ₁	1.87
SLDA	L ₂	2.81	SLDA	L ₂	2.37
	L ₃	2.81		L ₃	2.37
	L ₄	2.06		L ₄	1.62
For each additional L ₄ , add .50			For each additional L ₄ , add .50		
SRL	R ₁	1.81	SRL	R ₁	1.37
SRA	R ₂	1.56	SRA	R ₂	1.12
	R ₃	1.56		R ₃	1.12
	R ₄	1.56		R ₄	1.12
For each additional R ₄ , add .25			For each additional R ₄ , add .25		
SRDL	R ₁	2.56	SRDL	R ₁	2.12
SRDA	R ₂	2.31	SRDA	R ₂	1.87
	R ₃	2.06		R ₃	1.62
	R ₄	2.06		R ₄	1.62
	R ₅	3.31		R ₅	2.87
	R ₆	3.06		R ₆	2.62
	R ₇	2.81		R ₇	2.37
For each additional R ₄ , add .50			For each additional R ₄ , add .50		

MODEL 70

SLL	.2 (2 + F)
SLDL	.2 (3 + F)
SRL	.2 (2 + F)
SRDL	.2 (3 + F)
SLA	.2 (2 + F)
SLDA	.2 (3 + F)
SRA	.2 (2 + F)
SRDA	.2 (3 + F)

Where F = the number of shifts of eight bits required



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